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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/508,802	09/23/2004	Tomohisa Shiga	450100-04421	3919

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EXAMINER	
MOLL, JESSE R	
ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/508,802	SHIGA, TOMOHISA	
	Examiner	Art Unit	
	JESSE R. MOLL	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 14-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 14-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Withdrawn Rejections - 35 USC § 112

1. Applicant, via amendment, has overcome the rejection of claims 1-5 and 14-16 under 35 U.S.C. 112. The rejection is respectfully withdrawn.

2. Applicant, via amendment, has overcome the objection to the title. The objection is respectfully withdrawn.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patterson et al. () herein referred to as Patterson in view of 8051 Tutorial (8051 Tutorial: Addressing Modes; Vault Information Services; 2001) herein referred to as Vault.

5. Regarding claim 1, Patterson discloses an operation-processing device for performing operation processing based on an arbitrary operation program (program stored in Instruction memory; see figure 5.1), said device comprising: a register array having a plurality of registers each for holding an arbitrary value (Registers; see fig. 5.6 and 5.11; page 346, lines 2-3) based on a write address (Write register 1 and 2; see figure 5.6 and 5.11) and a write control signal (RegWrite; see figure 5.6) and outputting the held value (On Read data 1 and 2; see figure 5.6 and 5.11) to a signal line (Data line between Registers and ALU; see figure 5.11) based on a read address (Read register 1 and 2; see figure 5.6 and 5.11); an operation portion having an input coupled to said signal line (see Figure 5.11 regarding the input to the ALU), the operation portion being operable for performing an operation on a value read from said register array (ALU; see fig. 5.6 and 5.11) to said signal line (See Figure 5.11); an instruction-decoding portion for decoding an operation instruction from an operation program for operating said operation portion (decoding portion of Control; see fig. 5.19; see page 359); and an instruction-execution-controlling portion for controlling said register array and the operation portion in order to execute an operation instruction decoded by said instruction-decoding portion (Controlling portion of Control; see fig. 5.19; see page 359), wherein said instruction-execution-controlling portion selects one of said registers based on said operation instruction (using the rs and rt signals; see fig. 5.16);

Patterson does not expressly disclose that based on a value held by said selected register, said instruction-execution-controlling portion performs register-to-

register addressing processing for selecting another of said registers of said register array.

Vault teaches that based on a value held by said selected register (such as R0; see second page, Indirect Address section, first 5 paragraghs), said instruction-execution-controlling portion performs register-to-register addressing processing for selecting another register (register at the address that R0 holds; in this case, register at address 40h).

Note that the term register is broadly interpreted as any storage used by a computer (including RAM).

Because both references teach methods of addressing memory locations (registers), it would have been obvious to substitute the direct register addressing, as taught by Patterson, for indirect addressing, as taught by Vault to achieve the predictable results of accessing data from computer memory via register-to-register addressing.

6. Regarding claim 2, Patterson also discloses a read only memory cell in which said operation program is stored (see fig. 5.4 regarding providing only read access).

7. Regarding claim 3, the combination of Patterson and Vault would include operation instruction to perform the register-to-register addressing processing (shown in Vault; “MOV A,@R0”).

See above regarding claim 1 for a description of the combination.

8. Regarding claim 5, Patterson also discloses that said instruction execution-controlling portion has: a first selector for selecting any one of a read execution address (Read register 1; see fig. 5.6) a to select said one register and a read address to select this register again (the same address; if used in a next instruction, it will still select the same register); and a second selector for selecting any one of a write execution address (Write register 1; see fig. 5.6)to select said one register and a write address to select this register again (the same address);.

9. Claim 14 recites equivalent limitations as claim 1 with the exception listed below, which Patterson is obvious over Patterson in view of Vault.

Patterson teaches adding two registers (by the ALU; see figure 5.7) using direct addressing;

Patterson does not expressly teach performing operation on a value held by said selected another register and a value of the register selected register-to-register addressing processing.

Vault teaches using indirect addressing (see above regarding claim 1).

As stated above, it is obvious to combine indirect addressing with the system of Patterson. Using indirect addressing on an add instruction would yield performing operation on a value held by said selected another register and a value of the register selected register-to-register address processing (selected using indirect addressing).

10. Regarding claim 15, the combination of Patterson and Vault would include a result of said operation being stored in the register selected on the basis of the value held by said register (Clearly, the read register and write register can be equal).

11. Claim 16 recites equivalent limitations as claim 3 and is rejected for the same reasons.

12. Regarding claim 26, combination of Patterson and Vault would include at least one input signal line that is coupled to said signal line via a latch (see page 342 regarding clocking methodology; inherently if dataflow is controlled by a clock, data is stored in latches and therefore every data source is latched).

13. Claim 4 rejected under 35 U.S.C. 103(a) as being unpatentable over Patterson in view of Vault and common knowledge in the art. Examiner is taking Official Notice that the claim limitations stated in claim 4 were commonly known in the art at the time of the invention.

14. Regarding claim 4 Patterson also discloses that register array and the read only memory are comprised of plural memory cells (inherently, since the portions are addressable, there must be multiple “cells”).

15. Regarding claim 4 Patterson does not expressly disclose that said operation portion, the instruction-decoding portion, and the instruction-execution-controlling portion are comprised of plural arithmetic/logic operation elements; and wherein said

memory cells and the arithmetic/logic operation elements are constituted of a programmable logic devices formed on the identical semiconductor chip.

16. It was commonly known in the art to have the instruction-decoding portion, and the instruction-execution-controlling portion are comprised of plural arithmetic/logic operation elements; and wherein said memory cells and the arithmetic/logic operation elements are constituted of a programmable logic devices formed on the identical semiconductor chip.

17. All of the component parts are known in the art and Patterson and Vault. The only difference is the combination of "old elements" into a single device (device as shown in figure 1 and a single chip computer or microcontroller) by combining all elements onto a single chip.

18. Thus, it would have been obvious to one having ordinary skill in the art to combine the instruction-decoding portion, and the instruction-execution-controlling portion are comprised of plural arithmetic/logic operation elements; and wherein said memory cells and the arithmetic/logic operation elements onto a single programmable logic device. The functionality would be equivalent and the results would have been predictable.

Response to Arguments

19. Applicant's arguments filed 7 February 2008 have been fully considered but they are not persuasive. Regarding the argument that neither Patterson nor Vault teach

register-to-register addressing, Examiner disagrees. Vault teaches addressing a memory location (40h in the current rejection) based on a value held in another memory location (R0). Firstly, the term register is extremely broad and encompasses any memory location in a processor. Secondly, even if Vault does not teach the exact memory configuration as Patterson, it does not render the combination unobvious. Merely because a reference discusses addressing a certain type of memory in a particular fashion does not mean that it would not have been obvious to use the same addressing in another type of memory. The combination of the rejection above adds this type of addressing and does not but the external memory.

20. Regarding the argument that the limitations of claim 4 were not commonly known in the art, Examiner disagrees. Regarding the limitation "formed on an identical semiconductor chip", integrated circuits are extremely common and almost all modern processor are implemented on a single chip. ScienCentral shows evidence that integrated circuits were extremely well known at the time of the invention. Regarding the limitation "wherein said memory cells and the arithmetic/logic operation elements comprise a programmable logic device", field programmable gate arrays (FPGAs) were extremely commonly used to implement processors at the time of the invention. Zlotnick shows evidence that FPGAs were commonly used at the time of the invention (see background of the invention).

21. Added limitations are covered in the art rejection above.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse R. Moll whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 10:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571)272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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